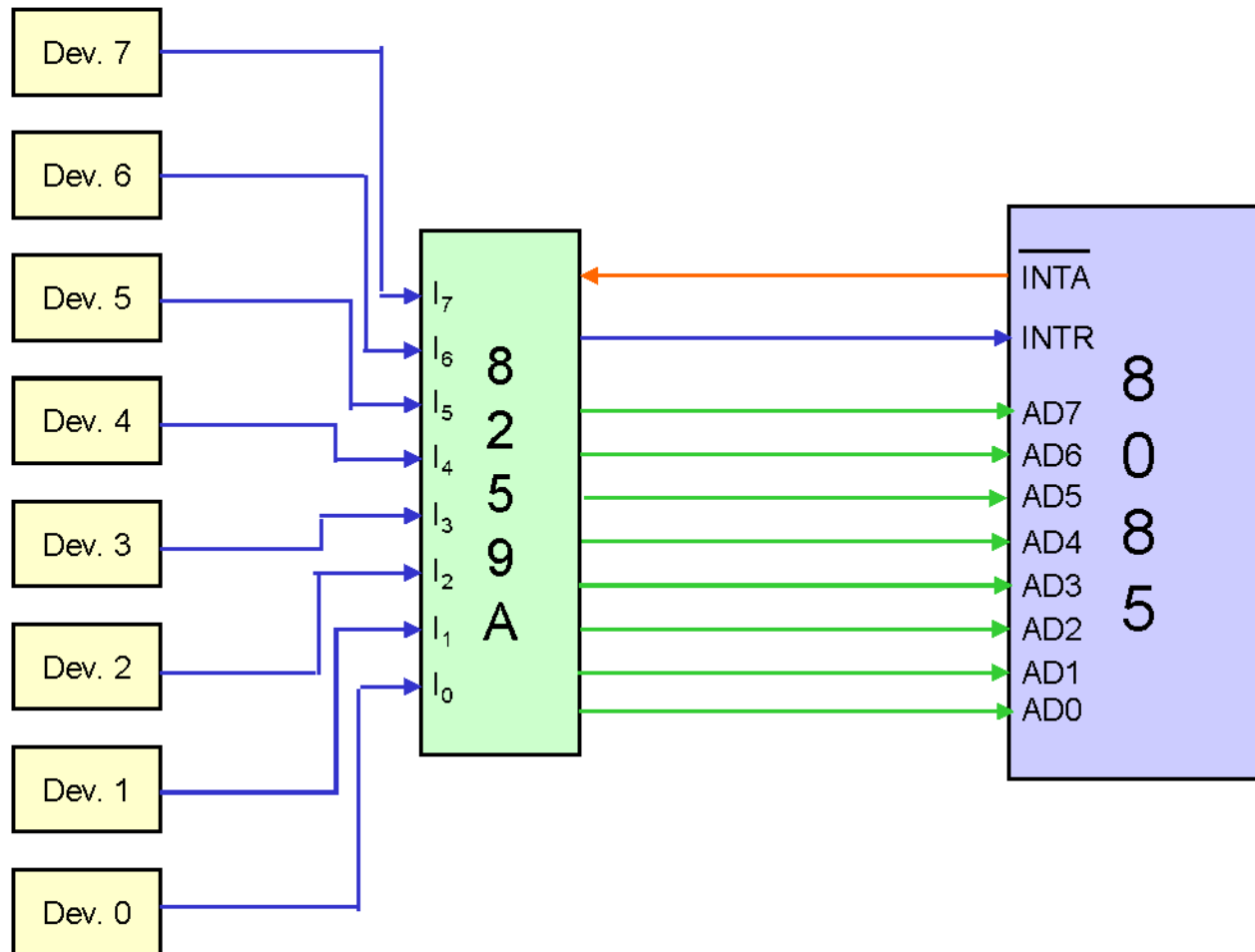


**Programmable Interrupt  
Controller  
8259A  
LECTURE 3**

# The Need for the 8259A

- The 8085 INTR interrupt scheme presented earlier has a few limitations:
  - The RST instructions are all vectored to memory page 00H, which is usually used for ROM.
  - It requires additional hardware to produce the RST instruction opcodes.
  - Priorities are set by hardware.
- Therefore, we need a device like the 8259A to expand the priority scheme and allow mapping to pages other than 00H.

# Interfacing the 8259A to the 8085



# Operating of the 8259A

- The 8259A requires the microprocessor to provide 2 control words to set up its operation. After that, the following sequence occurs:
  1. One or more interrupts come in.
  2. The 8259A resolves the interrupt priorities based on its internal settings
  3. The 8259A sends an **INTR** signal to the microprocessor.
  4. The microprocessor responds with an **INTA** signal and **turns off** the interrupt enable flip flop.
  5. The 8259A responds by placing the op-code for the **CALL instruction (CDH)** on the data bus.

# Operating of the 8259A

6. When the microprocessor receives the op-code for **CALL instead of RST**, it recognizes that the device will be sending **16 more bits** for the address.
7. The microprocessor sends **a second INTA** signal.
8. The 8259A sends the **high order byte** of the ISR's address.
9. The microprocessor sends **a third INTA** signal.
10. The 8259A sends the **low order byte** of the ISR's address.
11. The microprocessor executes the **CALL instruction** and jumps to the ISR.

# Direct Memory Access

- This is a process where data is transferred between two peripherals directly without the involvement of the microprocessor.
  - This process employs the HOLD pin on the microprocessor
    - The external DMA controller sends a signal on the HOLD pin to the microprocessor.
    - The microprocessor completes the current operation and sends a signal on HLDA and stops using the buses.
    - Once the DMA controller is done, it turns off the HOLD signal and the microprocessor takes back control of the buses.