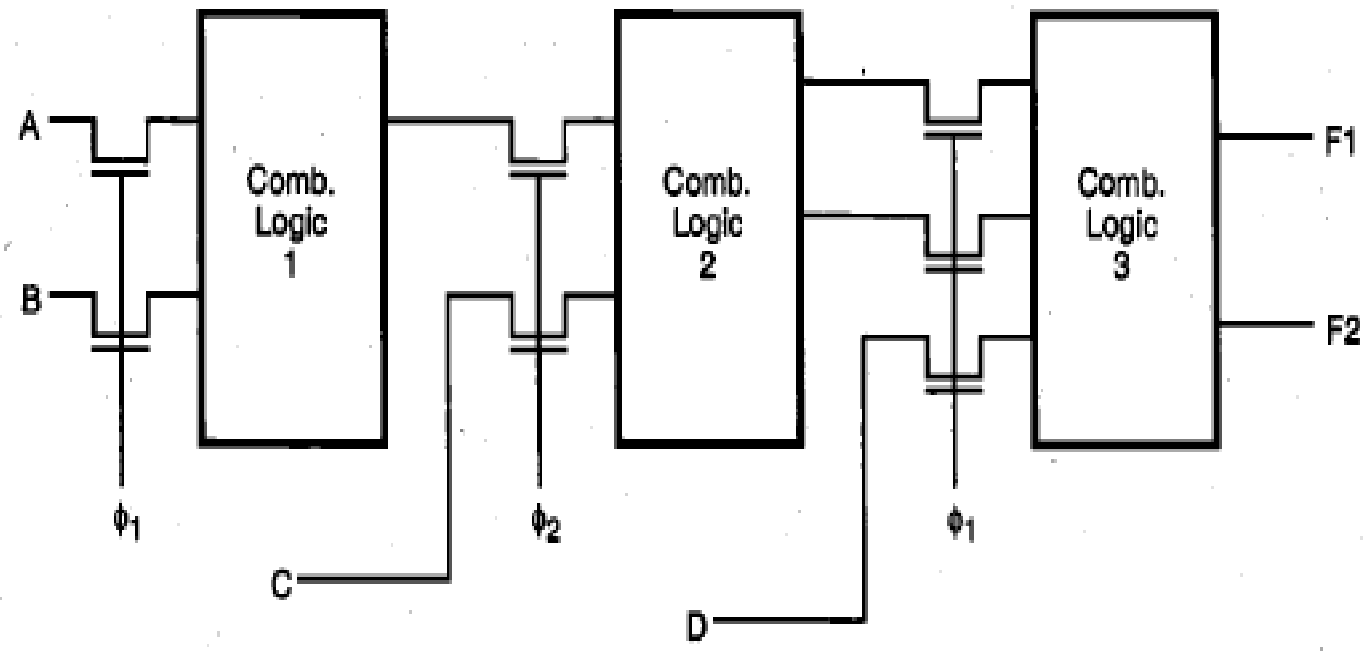
UNIT 4:
Dynamic logic circuits

Synchronous Dynamic Circuit Techniques

- **Dynamic Pass Transistor Circuits**



- The generalized view of a multi-stage synchronous circuit shown in Fig.
- The circuit consists of cascaded combinational logic stages, which are interconnected through nMOS pass transistors.
- All inputs of each combinational logic block are driven by a single clock signal.
- Individual input capacitances are not shown in this figure for simplicity, but the operation of the circuit obviously depends on temporary charge storage in the parasitic input capacitances

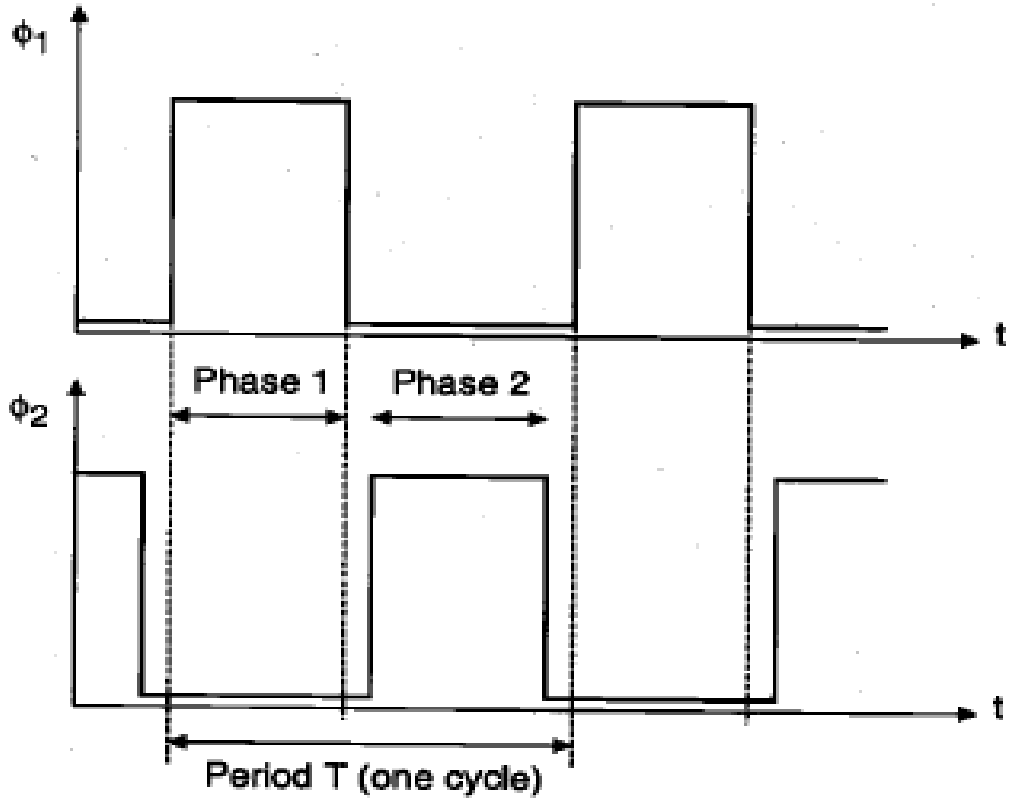


Fig. Nonoverlapping clock signals used for two-phase synchronous operation

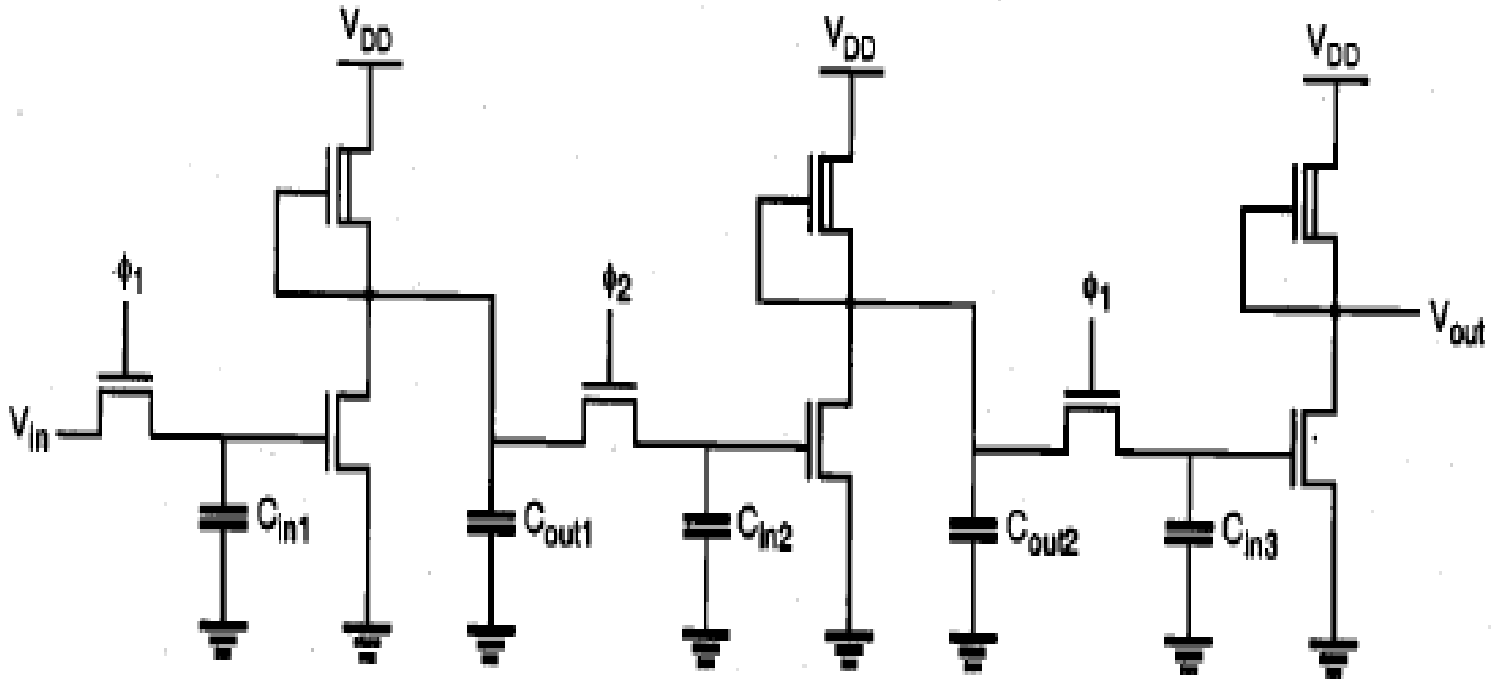


Fig. Three stages of a depletion-load nMOS dynamic shift register circuit driven with two-phase clocking.

CMOS Transmission Gate Logic

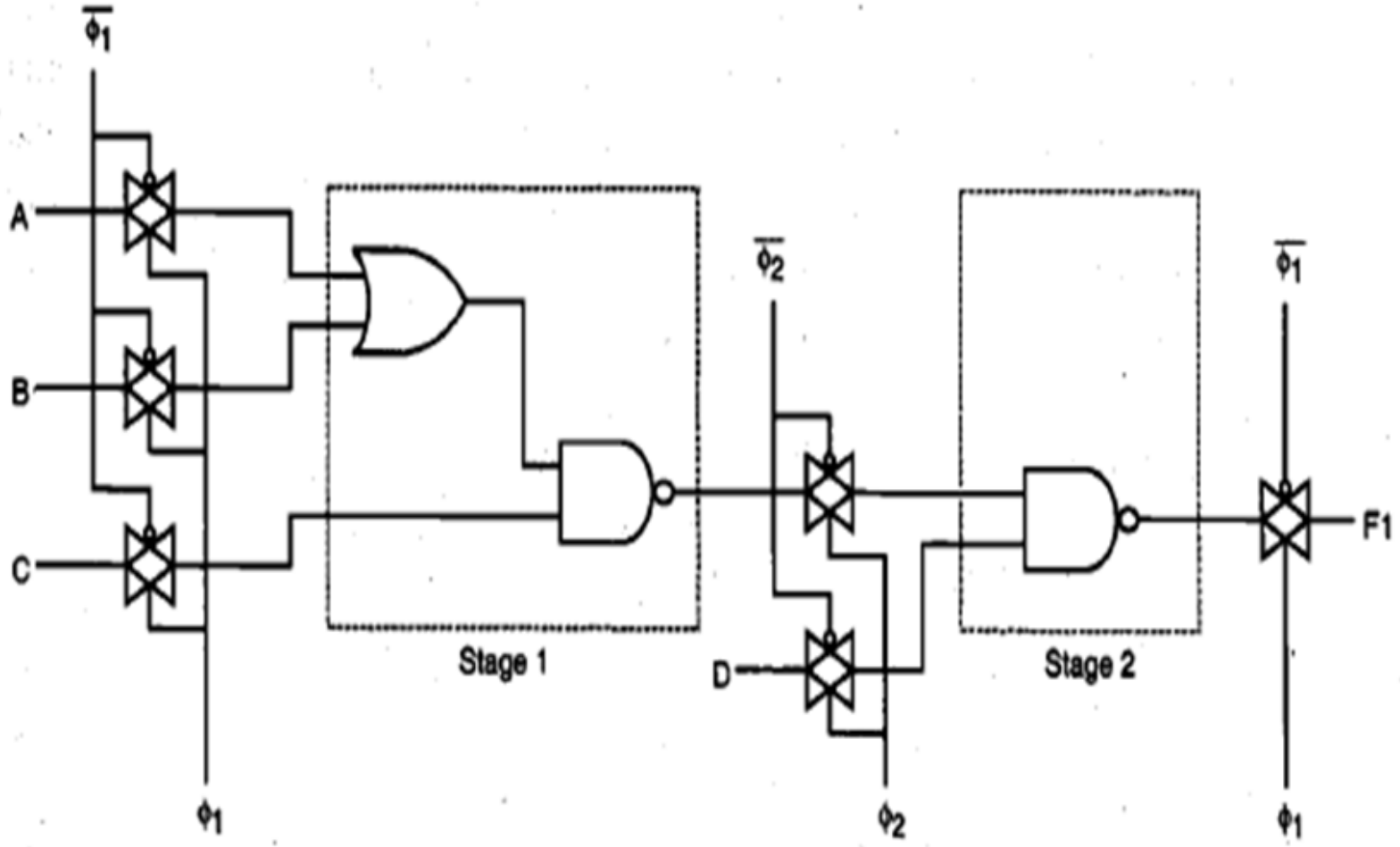
- The basic two-phase synchronous logic circuit principle, in which individual logic blocks are cascaded via clock-controlled switches, can easily be adopted to CMOS structures as well.

- Here, static CMOS gates are used for implementing the logic blocks, and CMOS transmission gates are used for transferring the output levels of one stage to the inputs of the next stage.

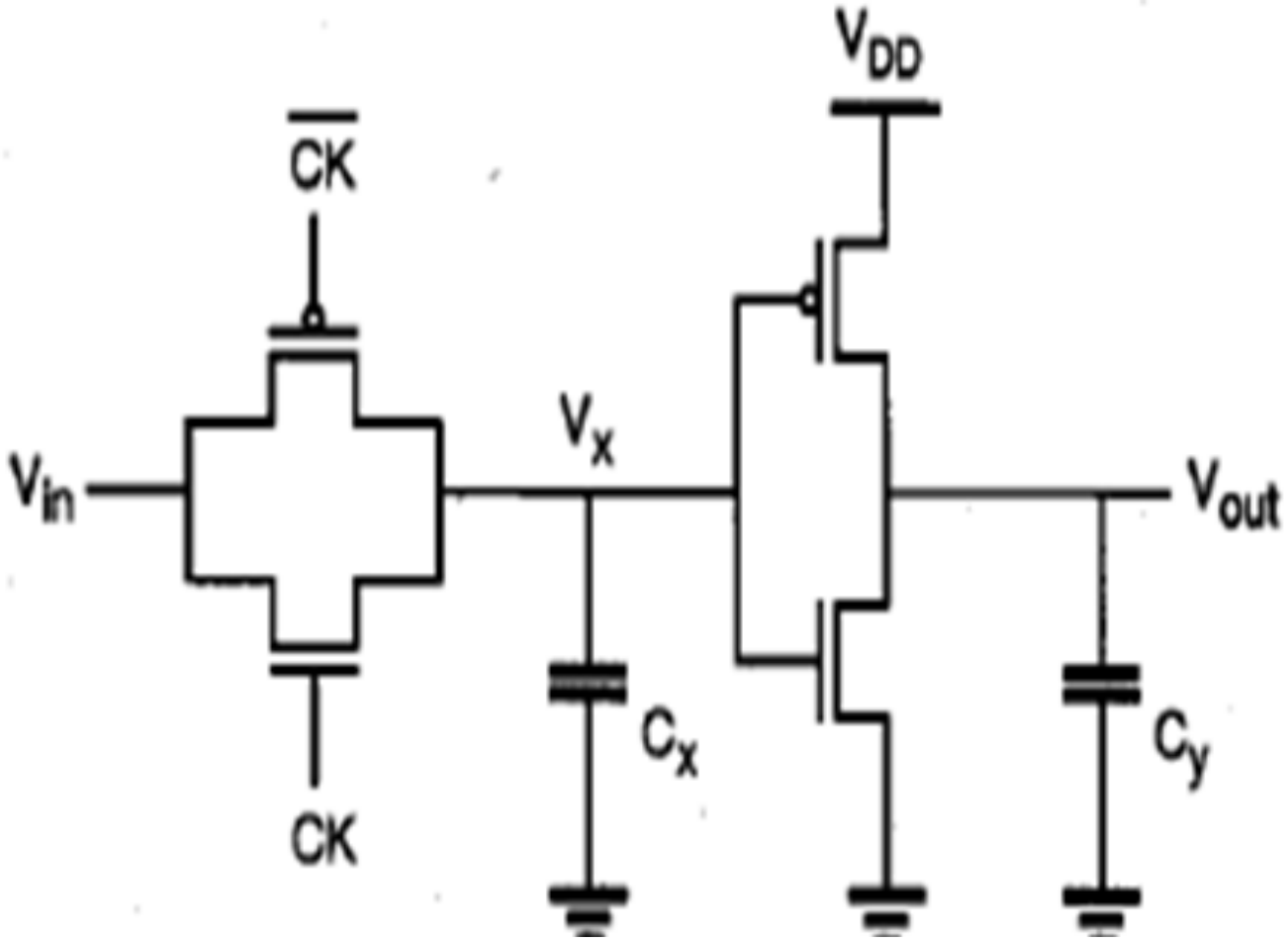
- Each transmission gate is actually controlled by the clock signal *and its complement.*

- *As a result, two-phase clocking in CMOS transmission* gate logic requires that a total of four clock signals are generated and routed throughout the circuit.

Typical example of dynamic CMOS transmission gate logic.



Basic building block of a CMOS transmission gate dynamic shift register



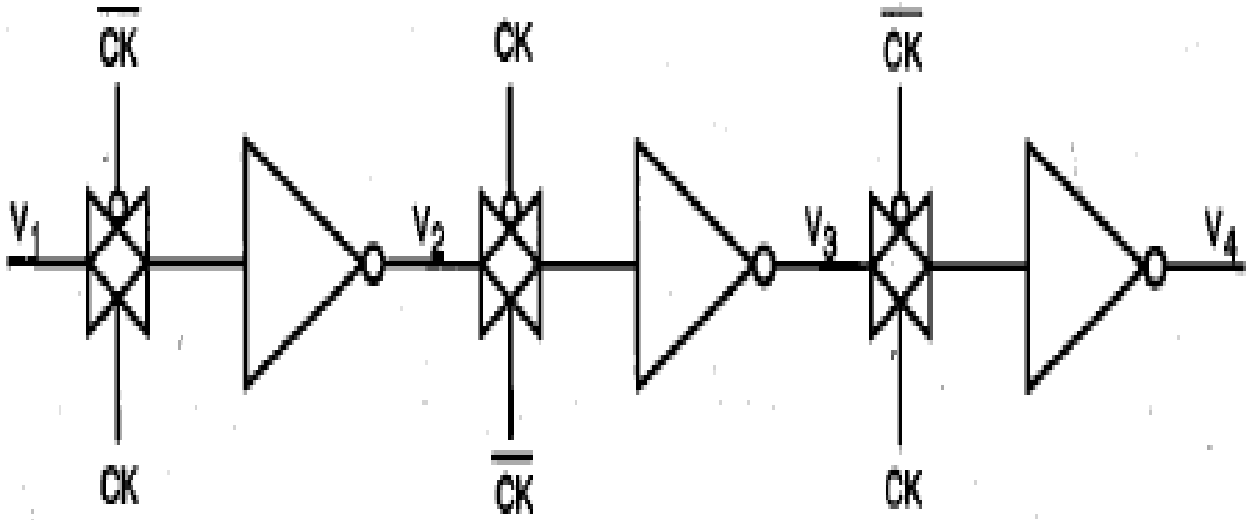
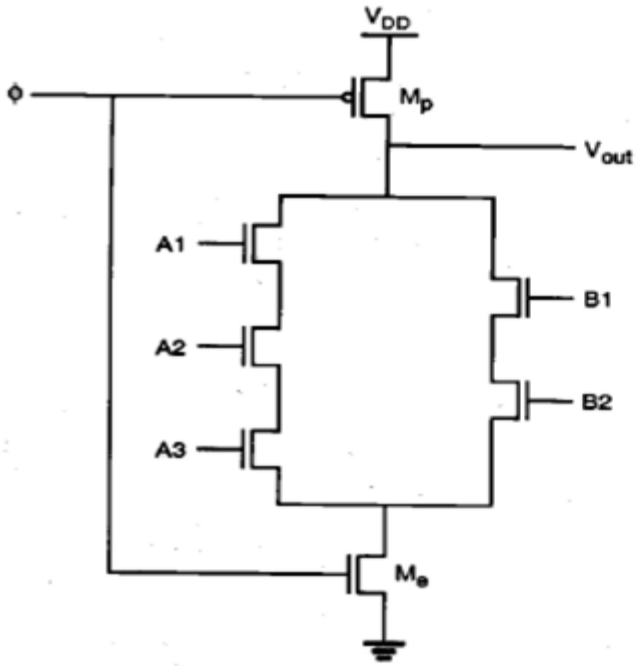


Fig. Single-phase CMOS transmission gate dynamic shift register

- ***Dynamic CMOS Logic (Precharge-Evaluate Logic)***



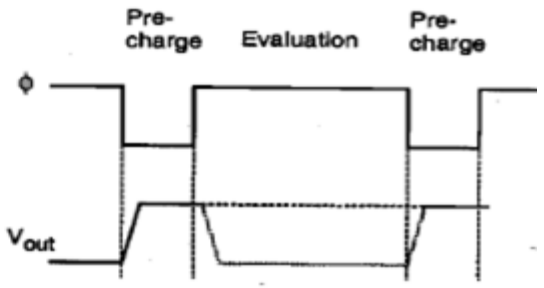


Illustration of the cascading problem in dynamic CMOS logic